Q8 OBC (On-Board Computer)

FEATURE HIGHLIGHTS

MODERN PERFORMANCE AND SPACE-PROVEN RELIABILITY

The On-Board Computer (OBC) is built around the Xiphos Q8 processor board, which offers 120+ years of flight heritage across 90+ missions. Xiphos' space-hardened COTS architecture has a record of no on-orbit board failures and low upset rates, as required for the core of your spacecraft. The AMO/Xilinx UltraScale+ MPSoC processor provides significant processing power, efficiency, and flexibility to meet the needs of your most demanding missions.

SPACECRAFT SUBSYSTEM CONTROL

The OBC offers a large selection of serial interfaces for all spacecraft subsystems, with options including RS-422/485, CAN, and LVDS-based protocols for ACS sensors and actuators, communications, propulsion, and EPS/thermal.

Gigabit Ethernet and USB 2.0 provide additional flexibility to support payload interfaces.

SPACECRAFT MONITORING

To monitor subsystems, the Q8 OBC provides -5V to +5V and 0V to 5V analog inputs, as well as PT2000 thermistor inputs for thermal monitoring.

FLEXIBILITY FOR YOUR MISSION

Your OBC should enable your spacecraft platform design, not limit it. The Xiphos toolchain gives you full control over the FPGA fabric and Linux Operating System environment.

Its reconfigurable 3v3 GPIO and LVDS pins allow for custom interfaces, while flexible RS-422/485 serial settings make it easy to adapt to your hardware suite.

Best of all, you can have it in any color you want - as long as it's silver.

APPLICATIONS

The flexibility of the Q8 OBC, along with its modest SWaP requirements, make it ideally suited for MicroSat and SmallSat buses.
Extensive 1/0, processing, and storage resources for bus Sufficient payload resources without separate interface box 30krad TID for long-duration missions
Low upset rate of the Xilinx UltraScale+

ROBUSTNESS FEATURES FOR YOUR SPACECRAFT

- Triple mode redundancy in Control FPGA
- EDAC-protected RAM
- Upset and multi-current monitoring
- Overcurrent protection (multiple)
- FPGA bit-stream scrubbing
- Software robustness/ watchdog

SOFTWARE DEVELOPMENT

To support software development on Linux workstations, Xiphos provides an Application Development Kit, with standard Linux libraries for CIC++. If you've previously developed code for Linux desktop and server applications, you can easily port it to the OBC. Access OBC hardware and logic interfaces through standard Linux and Xilinx kernel drivers or custom drivers provided by Xiphos.

LOGIC DEVELOPMENT

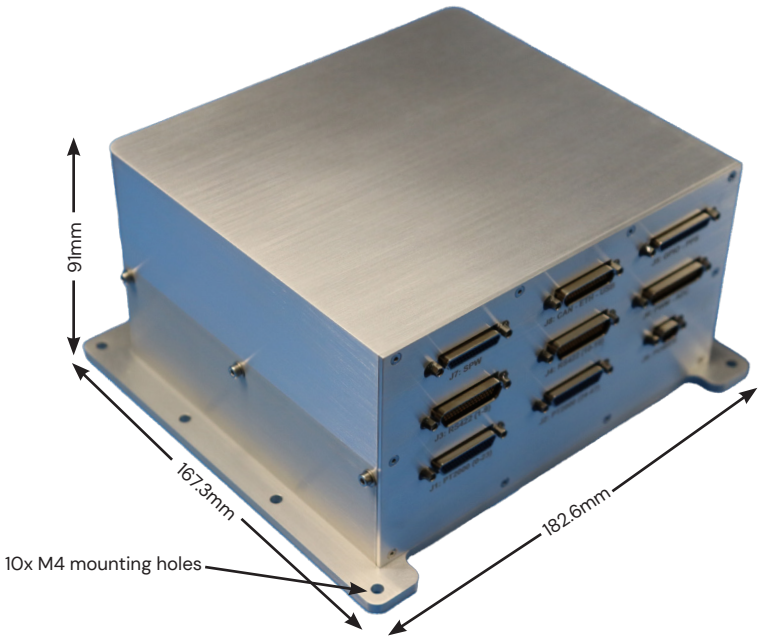
Logic development uses standard Xilinx development tools. Xiphos, Xilinx, and many third party vendors also provide a wide range of compatible reusable logic cores for Xilinx FPGAs.

FLIGHT HERITAGE

The OBC solution's maiden flight is scheduled for 2025, built on the extensive flight heritage of the Q8 processor:

Other flight heritage products in the current Xiphos Q-Card family include the Q7, Q8, and Q8J.

Over 210 Q-Cards have flown to date, and Xiphos has been flying prior generations of the Xiphos Q-Card family since 2002.



CHARACTERISTICS

COMMUNICATION INTERFACES

- 1x GigE (1Gbps) port with magnetics
- 2x USB 2.0
- 2x CAN bus (2.0B)
- 2x UART over CAN [PHY]
- 18x RS422/485/232 ports
- 2x RS422/485/232 ports [Full Duplex only]
- 7x RS422 OUT ports
- 1x RS422/485/232 Remote Diagnostic Port (RDP)
- 1x Power cycle request input

CONFIGURABLE INTERFACES

- 6x LVDS outputs
- 6x LVDS inputs
- 10x 3.3V outputs
- 10x 3.3V inputs

ANALOG INTERFACES

- 9x Analog inputs (0 to 5V, 10mV accuracy)
- 3x Analog inputs (-5 to 5V, 20mV accuracy

TEMPERATURE INTERFACES

- 48x PT2000 Temperature sensors Inputs

FORM FACTOR

- 167.3 mm x 182.6 mm x 91 mm
- 957 g

ENVIRONMENTAL

- Operating Temperature -40 to +60C

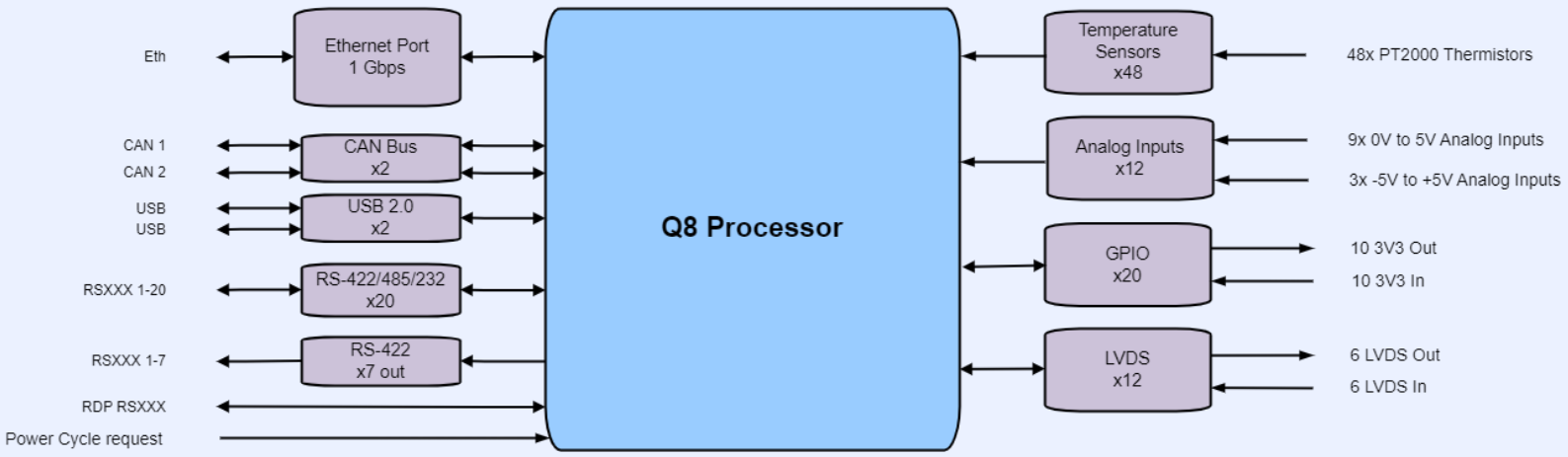
POWER CONNECTOR

- J9 Micro-D 9 Socket
- Input voltage: 9 to 15V (12V nominal)
- 7.5W nominal and 14W peak

I/O CONNECTORS

- J1 Micro-D 51 pins - 24x PT2000 inputs
- J2 Micro-D 51 pins - 24x PT2000 inputs
- J3 Micro-D 51 pins - 8x RSXXX ports
  1x RSXXX Remote Diagnostic Port (RDP)
- J4 Micro-D 51 pins - 10x RSXXX ports
- JS Micro-D 37 pins - 2Ox 3V3 GPIO (10 + 10)
  2x RS422 [Full Duplex only]
  1x Power cycle request input
- J6 Micro-D 37 pins - 12x Analog inputs
  6x RS422 out
- J7 Micro-D 51 pins - 12x LVDS pairs
- J8 Micro-D 31 pins - 2x CAN bus
  2x UART over CAN PHY
  1x Ethernet
  2x USB ports

BLOCK DIAGRAM



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